wherein conductive attachment elements 16 have been attached thereto. Interposer 12 includes a plurality of layers having routing lines and vias therein which serve as electrical conductors. One set of conductors, depicted as conductors 50, 52, 54 and 56, pass through interposer 12 and serve to electrically connect pads 26 of chips 24 to the contact pads 22 of interposer 12. These conductors are selected to have suitable conductivity and may be, for example, aluminum or copper. Interposer 12 also includes a set of testing conductors, depicted as conductor 58, that pass through interposer 12 connecting some of the contact pads 26 of chips 24 to a testing apparatus as will be explained in greater detail below. The testing conductors may provide direct electrical connection to the testing apparatus or may pass through a multiplexer or other intervening apparatus (not shown) incorporated into interposer 12.

Please replace the paragraph on page 17, line 7-19 with the following paragraph:

For example, as best seen in figure 3B, interposer 32, which has conductive attachment elements 36 attached thereto, includes a plurality of layers having routing lines and vias therein which serve as electrical conductors. One set of conductors, depicted as conductors 60, 62, 64 and 66 pass through interposer 32 to

electrically connect contact pads 42 on the upper surface of interposer 32 to contact pads 46 on chips 44 (see figure 2). Another set of conductors, depicted as conductors 68 and 70, are testing conductors that pass through interposer 32 and are used to connect certain pads 46 of chips 44 (see figure 2) to a testing apparatus, as will be explained in greater detail below. As such, the geometry of pads 42 on the upper surface of interposer 32 is different from that of pads 46 on chips 44.

In the Claims

The Applicant has presented all of the pending claims for the Examiner's convenience with claims 1-13, 18-30, 36 and 41 being amended.

1. (Amended) A method for selecting components for a matched set comprising the steps of:

electrically and mechanically coupling a semiconductor wafer having a plurality of integrated circuit chips to an interposer to form a wafer-interposer assembly;

simultaneously testing at least two of the integrated circuit chips of the semiconductor wafer;

dicing the wafer-interposer assembly into a plurality of chip assemblies; and